PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent No. 6,897,531 B2	)	Serial No. 10/617,737
Inventor(s): Takashi OHSAWA	)	Filed: July 14, 2003
Issue Date: May 24, 2005	)	Attorney Docket No. 002372.00045

For: SEMICONDUCTOR MEMORY DEVICE

REQUEST FOR CERTIFICATE OF CORRECTION

U.S. Patent and Trademark Office
Customer Service Window
Randolph Building, Mail Stop: Certificate of Correction Branch
401 Dulany Street
Alexandria, VA 22314

Sir:

Pursuant to 35 U.S.C. § 254 and 37 C.F.R. § 1.322, this is a request for the issuance of a Certificate of Correction in the above-identified patent. Two (2) copies of PTO Form 1050 are appended. The complete Certificate of Correction involves one page.

The mistakes identified in the appended Form occurred through no fault of the Applicant, as clearly disclosed by the records of the application, which matured into this patent. Enclosed for your convenience is the relevant portion of the Amendment filed November 15, 2004.

Issuance of the Certificate of Correction containing the corrections is respectfully requested. Since these changes are necessitated through no fault of the Applicant, no fee is believed to be associated with this request. Nonetheless, should the Patent and Trademark Office determine that a fee is required, please charge our Deposit Account No. 19-0733.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Dated: January 13, 2006

By: _____
Gary D. Fedorochko
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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 6,897,531 B2

DATED: May 24, 2005

INVENTOR(S): Takashi OHSAWA

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 16, Claim 1, Line 63:
Please replace "ton" with --top--

In Column 17, Claim 2, Line 29:
Please replace "sates" with --gates--

Mailing Address of Sender:

Banner & Witcoff, Ltd.
11th Floor
1001 G Street, N.W.
Washington, DC 20001-4597

FORM PTO 1050 (Rev.2-93)

U.S. PAT. NO 6,897,531

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UNITED STATES PATENT AND TRADEMARK OFFICE

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FORM PTO 1050 (Rev.2-93)

U.S. PAT. NO 6,897,531

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JAN 20 2006

☒ PATENT ☐ DESIGN B&W Ref. 002372.00045 Date: 11-15-04

☐ HAND CARRY Group/Section _____ Bldg _____ Rm _____

Serial/Patent No.: 10/617737 Atty/Sec: GDF/lab

Inventor: OHSAWA Client: Kyowa

Title: _____

The following has been received in the U.S. Patent and Trademark Office on the date stamped hereon:

☐ _____ total pp Spec., including : # of Claims _____
# of independent claims _____ ☐ Abstract
☐ Application Data Sheet (ADS): ☐ Initial ☐ Supplemental
☐ Drawings: ☐ Formal ☐ Informal
# of distinct sheets _____ Figs: _____
☐ Nonpublication Request
☐ Declaration/Power of Attorney: ☐ Executed ☐ Unexecuted
☐ Assignment w/PTO Cover Sheet
☐ IDS w/PTO 1449 ☐ References ☐ w/Fee
☐ Preliminary Amendment
☐ Priority Claim: (Foreign or U.S. Provisional) B&W# _____
Country Appl. # Date
☐ w/Foreign Priority Document(s)
☐ Application: ☐ CIP ☐ Continuation ☐ Divisional
Parent SN: _____ B&W# _____
☐ U.S. Provisional _____ pp Spec/Claims; Cover Sheet
☐ Response to Missing Parts/Requirements dtd _____
☐ Response to Notice to File Corrected Appln. Papers dtd _____
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☐ Request for Corrected : ☐ Filing Receipt ☐ Assignment
☐ Response to Restriction/Election Requirement
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☐ Request for Approval of Drawing Changes
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OIPE SC174 NOV -1-5-2004 PATENT & TRADEMARK OFFICE

B&W Rev. 01/04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:		Atty. Docket No.:	002372.00045
Takashi OHSAWA			
Serial No.:	10/617,737	Group Art Unit:	2815
Filed:	July 14, 2003	Examiner:	Wilson, A.
For:	SEMICONDUCTOR MEMORY DEVICE	Confirmation No.:	3632

AMENDMENT

U.S. Patent and Trademark Office
220 20th Street S.
Customer Window, Mail Stop Amendment
Crystal Plaza Two, Lobby, Room 1B03
Arlington, VA 22202

Sir:

In response to the Office Action mailed September 7, 2004, please amend the instant application as follows:

Amendments to the Claims are reflected in the Listing of Claims, which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

An **Appendix** including amended drawing figures is attached following page 7 of this paper.

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-5 (canceled)

Claim 6 (currently amended): A ~~The~~ semiconductor memory device ~~according to claim 4,~~ having full depletion type MISFETs to constitute memory cells on a semiconductor substrate via an insulating film, each of the MISFETs comprising:

a semiconductor layer formed on the insulating film;

a source region formed in the semiconductor layer;

a drain region formed apart from the source region in the semiconductor layer, the semiconductor layer between the source region and the drain region serving as a channel body in a floating state;

a main gate formed on a first side of the channel body to form a channel in the channel body; and

an auxiliary gate formed on a second side of the channel body, the second side being opposite to the first side, a portion of the second side of the channel body being capable of accumulating majority carriers under conditions in which the channel body is fully depleted by an electric field from the main gate and an electric field is applied to the channel body from the auxiliary gate,

wherein the MISFET has a first data state in which the majority carriers are accumulated in the portion of the second side of the channel body and a second data state in which the majority carriers accumulated in the portion of the second side of the channel body are emitted,

wherein the MISFETs are arranged in the form of a matrix to constitute a cell array, the drain regions are connected to bit lines, the main gates constitute word lines intersecting the bit lines, the source regions are connected to a fixed potential line and the auxiliary gate is formed as a common electrode shared among the memory cells.

wherein the first side of the channel body is a top side face of the semiconductor layer, the second side of the channel body is a back side face of the semiconductor layer and the main gate is formed on the top side face via a gate insulating film, and

wherein the auxiliary gate is an impurity doping layer buried between the semiconductor substrate and the insulating film.

Claim 7 (canceled)

Claim 8 (currently amended): A ~~The~~ semiconductor memory device ~~according to claim 1,~~ having full depletion type MISFETs to constitute memory cells on a semiconductor substrate via an insulating film, each of the MISFETs comprising:

a semiconductor layer formed on the insulating film;

a source region formed in the semiconductor layer;

a drain region formed apart from the source region in the semiconductor layer, the semiconductor layer between the source region and the drain region serving as a channel body in a floating state;

a main gate formed on a first side of the channel body to form a channel in the channel body; and

an auxiliary gate formed on a second side of the channel body, the second side being opposite to the first side, a portion of the second side of the channel body being capable of accumulating majority carriers under conditions in which the channel body is fully depleted by an electric field from the main gate and an electric field is applied to the channel body from the auxiliary gate,

wherein the MISFET has a first data state in which the majority carriers are accumulated in the portion of the second side of the channel body and a second data state in which the majority carriers accumulated in the portion of the second side of the channel body are emitted,

wherein the MISFETs are arranged in the form of a matrix to constitute a cell array, the drain regions are connected to bit lines, the main gates constitute word lines intersecting the bit lines, the source regions are connected to a fixed potential line and the auxiliary gate is formed as a common electrode shared among the memory cells, and